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**ELECTROSTATIC DISCHARGE PROTECTIVE  
CIRCUITRY EQUIPPED WITH A COMMON  
DISCHARGE LINE**

**BACKGROUND OF THE INVENTION**

This application is a continuation-in-part of U.S. patent  
10 application Ser. No. 09/396,164, filed September 14, 1999.

**1. Field of the Invention**

15 The present invention relates to a semiconductor device, and more particularly, to a semiconductor device having an electrostatic discharge protective circuitry adapted to a common discharge line (CDL).

20 **2. Description of the Prior Art**

Electrostatic discharge, ESD hereafter, is a common phenomenon that occurs during handling of semiconductor IC devices.  
25 An electrostatic charge may accumulate for various reasons and cause potentially destructive effects on an IC device. Damage typically can occur during a testing phase of its fabrication, during assembly of the IC onto a circuit board, as well as during use of equipment into which

the IC has been installed. Damage to a single IC due to poor ESD protection in an electronic device can hamper some of its designed functions, or sometimes all of them. ESD protection for semiconductor ICs is, therefore, a reliability problem. In order to prevent this, various electrostatic breakdown protection techniques have been proposed. As one such technique discloses, Japanese Patent Application Kokai Publication No. Hei 7-086510 is a semiconductor device that is equipped with a common discharge line (CDL).

The conventional design for preventing ESD damage is a prodigious network that, for the most part, involves locating a protection circuit between the input/output pads and the V<sub>sub</sub>.SS terminal, between the input/output pads and the V<sub>sub</sub>.DD terminal, and between the V<sub>sub</sub>.SS and V<sub>sub</sub>.DD power rails. Accordingly, such a prodigious network consumes a great amount of layout area, especially when used in a configuration including multi-power buses. Moreover, no ESD protection is provided between any two IC pads using the conventional design. Thus, ESD stress arising between two IC pads is only indirectly bypassed via the protection circuit located between the V<sub>sub</sub>.SS and V<sub>sub</sub>.DD power rails.

However, the ESD pulse will boost the electric potential at the power rails, resulting in potential damage to the internal circuitry. K. Narita et al. have proposed another ESD protection circuit design in their article entitled "A NOVEL ON-CHIP ELECTROSTATIC DISCHARGE (ESD) PROTECTION FOR BEYOND 500 MHz DRAM," IEDM Proceeding, 1995, pp. 539-542. However, this design also features a common discharge line as a discharge path.

FIG. 1A shows a conventional gate-grounded NMOS field-effect transistor that is commonly used in ESD protection circuit design, wherein its gate electrode is tied to its source electrode at node 10 and connected to the ground, GND. The current-voltage, I-V, characteristics of the gate-grounded NMOS field-effect transistor is shown in FIG. 1B, referring to what is shown in FIG. 1B, the voltage V across the drain and source electrode of the gate-grounded NMOS field-effect transistor, shown in FIG. 1A, is greater than the threshold voltage  $V_{th}$ , referring to point A, the gate-grounded NMOS field-effect transistor is then triggered. The gate-grounded NMOS field-effect transistor snapback at point B where the voltage V reaches  $V_{sb}$  value, moreover, it enters the second breakdown region at point C where the voltage V is at  $V_{z2}$  value. Once the gate-grounded NMOS field-effect transistor enters the second breakdown region, thermal runaway will occur, hence easily result in device damages.

The gate-grounded NMOS field-effect transistor combines with a diode to form an ESD protection circuit that features a common discharge line as a discharge path. The overall ESD protection circuit for this particular example is shown in FIG. 1C. The protection circuit between any two pads is schematically depicted, wherein the circuit between Pad 1 and Pad 2 is shown by way of example. When an ESD stress having a positive polarity with respect to Pad 1 arises at Pad 2, the associated ESD voltage is coupled to a gate-grounded NMOS field-effect transistor  $N_2$ , and thus triggers the NMOS field-effect transistor  $N_2$  to be operated in snapback mode. Consequently, a great amount of ESD discharge current  $I_1$  flows from Pad 2, through a

common discharge line 30, to Pad 1, because the diode D<sub>1</sub> is forward biased.

- Conversely, when an ESD stress having a negative polarity with respect to Pad 1 arises at Pad 2, the associated ESD voltage is coupled to a gate-grounded NMOS field-effect transistor N<sub>1</sub>, and thus triggers the NMOS field-effect transistor N<sub>1</sub> to be operated in snapback mode. Consequently, a great amount of ESD discharge current I<sub>2</sub> flows from Pad 1, through the common discharge line 30 and then to Pad 2, because the diode D<sub>2</sub> is forward biased. This symmetrical characteristic of discharge path in accompanies with the simplification in ESD protection design contributes to the advantages of using CDL structure in ESD protection design.
- Nevertheless, the triggering voltage of using a gate-grounded NMOS field-effect transistor and a diode as ESD elements in between a Pad and the common discharge line is too high to protect submicron IC devices in the conventional method. Moreover, as mentioned earlier, once the gate-grounded NMOS field-effect transistor enters the second breakdown region, thermal runaway is likely to occur, hence easily result in device damages. Furthermore, ESD protection by using the conventional method is easily restricted in CMOS process, this is because the channel length of the gate-grounded NMOS field-effect transistor needs to be smaller than the output NMOS for making sure the gate-grounded NMOS field-effect transistor breakdown before the output NMOS.

It is therefore an object of the present invention to provide an enhanced ESD protection performance apparatus, which is equipped with a common discharge line, for protecting VLSI circuits and  
5 particularly CMOS devices.

### SUMMARY OF THE INVENTION

10 An object of the present invention is to substantially obviate one or more of the problems caused by limitations and disadvantages of the related art.

Another object of the present invention is to provide an ESD  
15 protection network having a triggering voltage and a holding voltage lower than that of the conventional design, which can effectively make submicron IC devices immune to ESD damage.

A further object of the present invention is to provide an enhanced ESD protection performance apparatus, which is equipped  
20 with a common discharge line, for protecting VLSI circuits and particularly CMOS devices.

In accordance with the present invention, there is provided a  
25 semiconductor device having an electrostatic discharge protective circuitry adapted to a common discharge line (CDL). In the embodiments of the present invention, the semiconductor device includes a plurality of bonding pads, each having at least a terminal, a

common discharge line, and a protective device connected between the terminal of at least one bonding pad and the common discharge line. Moreover, the protective device includes a thyristor, typically a silicon-control-rectifier, used for electrostatic discharge protection and 5 a triggering device, typically a zener diode, for lowering a trigger voltage of the thyristor.

#### BRIEF DESCRIPTION OF THE DRAWINGS

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The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIG. 1A schematically depicts a gate-grounded NMOS FET which is conventionally used as an ESD protection element;

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FIG. 1B shows the I-V characteristics of the gate-grounded NMOS field-effect transistor of FIG. 1A;

FIG. 1C schematically depicts a conventional CDL ESD protection circuitry between any two IC Pads;

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FIG. 2A and FIG. 2B schematically depicts a low triggering voltage SCR having a zener diode trigger in two different arrangements;

FIG. 2C shows the I-V characteristics of the low triggering voltage SCR of both FIG. 2A and FIG. 2B;

5 FIG. 2D shows the connection between the zener diode and the PNP transistor in the CMOS process;

10 FIG. 3 schematically depicts a modified CDL ESD protection circuitry of an embodiment of the present invention; and

15 FIG. 4 schematically depicts a modified CDL ESD protection circuitry of another embodiment of the present invention.

## **DESCRIPTION OF THE PREFERRED EMBODIMENT**

Before describing details of the present invention, a low triggering voltage SCR serves as the main component in an ESD protection circuit will be first described with reference to FIG. 2A and FIG. 2B. In both the drawings, the SCR device consists essentially of a PNP bipolar junction transistor T.sub.1 and an NPN bipolar junction transistor T.sub.2. The collector of the PNP transistor T.sub.1 is connected together with the base of the NPN transistor T.sub.2, forming a cathode gate identified by the node 200. The cathode gate 200 is coupled to the emitter of the NPN transistor T.sub.2, via a spreading resistor R.sub.a, constituting a cathode 201, which is connected to a ground terminal GND. The base of the PNP transistor

T.sub.1 is connected together with the collector of NPN transistor T.sub.2 to form an anode gate identified by the node 202. The anode gate 202 is coupled to the emitter of the PNP transistor T.sub.1 via a spreading resistor R.sub.b, constituting an anode 203. To achieve a

- 5 reduction of the SCR triggering voltage from about 30-50 volts to a level of about 5-10 volts, a zener diode Z.sub.1 is incorporated in the SCR device as a trigger. The zener diode Z.sub.1 can be placed in between the anode 203 and the cathode gate 200, like what is shown in FIG. 2A, or in between the anode gate 202 and the cathode 201, like  
10 what is shown in FIG. 2B. No matter of which, when either transistor is triggered to turn ON, it turns ON the other and both stay ON until the current is interrupted. As noted above, the SCR is an ideal device for on-chip protection against ESD since in its ON state it protects sensitive devices by virtue of its comparatively low resistance. In this  
15 invention, the PNP bipolar junction transistor T.sub.1 of the SCR device can connect with the zener diode Z.sub.1 in the CMOS process, as shown in FIG.2D. Because the SCR device comprise the zener diode Z.sub.1, it is not necessary that the SCR device combines with a diode, and that the zener diode Z.sub.1 is not additional, it must be  
20 connected with the PNP bipolar junction transistor T.sub.1 to form the SCR device, wherein anode 203 is connected with a N+ junction and one of P+ junctions of T.sub.1, and another P+ junction of T.sub.1 is formed by way of using additional implantation.

- 25 FIG. 2C shows the I-V characteristics of the low triggering voltage SCR with zener diode depicts in both FIG. 2A and 2B. Referring to FIG. 2C, one can see that when the voltage V across the anode and the cathode of the low triggering voltage SCR of both FIG. 2A and 2B is

greater than the threshold voltage  $V_{th}$ . Referring to point D, the SCR  
is then triggered. Sequentially, a low-holding voltage  $V_h$  is generated at  
point E, and since the low-holding voltage  $V_h$  is quite low, the resulting  
power consumption is small. In the mean while, using zener diode as a  
5 triggering element makes the SCR have a much lower triggering voltage  
at point D as compared to the conventional element at point A.

FIG. 3 schematically depicts a semiconductor device with a modified CDL (Common Discharge Line) ESD (Electrostatic Discharge)  
10 protection circuitry of an embodiment of the present invention, which  
utilizes the low triggering voltage SCR with zener diode as depicted in  
FIG. 2A. The semiconductor device comprises a plurality of bonding  
pads 300, 310 and 320, possibly a mixture of input pads, output pads,  
V.<sub>sub</sub>DD pads, and/or V.<sub>sub</sub>SS pads, each having at least one  
15 connecting terminal 301, 311 and 321; a common discharge line 330  
with open-ended design. That is, neither grounded nor connected to  
any source; and a protective device 302, 312 and 322 connected  
between the connecting terminal of at least one bonding pad and the  
common discharge line. The protective devices 302, 312 and 322 each  
20 includes a silicon-control-rectifier used for electrostatic discharge  
protection and a zener diode Z.<sub>sub</sub>1, Z.<sub>sub</sub>2 and Z.<sub>sub</sub>n for lowering  
a trigger voltage of the silicon-control-rectifier.

Moreover, the silicon-control-rectifier composes of a PNP  
25 bipolar transistor T.<sub>sub</sub>11, T.<sub>sub</sub>12 and T.<sub>sub</sub>1n with an emitter 303,  
313 and 323 connected to the connecting terminal of at least one  
bonding pad. A NPN bipolar transistor T.<sub>sub</sub>21, T.<sub>sub</sub>22 and  
T.<sub>sub</sub>2n with an emitter 304, 314 and 324 connected to the common

discharge line 330. A first resistor R.sub.a1, R.sub.a2 and R.sub.an with a first end 305, 315 and 325 connected to a collector of the PNP bipolar transistor and a base of the NPN bipolar transistor. It also includes a second end connected to the common discharge line 330 and a second resistor R.sub.b1, R.sub.b2 and R.sub.bn with a first end connected to the connecting terminal of at least one bonding pad. Further shown is a second end 306, 316 and 326 connected to a base of the PNP bipolar transistor and a collector of the NPN bipolar transistor.

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- The zener diodes Z.sub.1, Z.sub.2 and Z.sub.n of the present embodiment are placed across the emitters and the collectors of the PNP bipolar transistors T.sub.11, T.sub.12 and T.sub.1n, that is anodes of the zener diodes are connected to the connecting terminals 301, 311 and 321 and cathodes of the zener diodes are connected to the first end 305, 315 and 325 of the first resistor R.sub.a1, R.sub.a2 and R.sub.an.

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- Furthermore, when the bonding pad 300 positive stress to the bonding pad 310, the discharge way is from the PNP bipolar transistor T.sub.11 and the zener diode Z.sub.1 through common discharge line 330 to the first resistor R.sub.a2 and the zener diode Z.sub.2. On the contrary, when the bonding pad 300 negative stress to the bonding pad 310, the discharge way is from the PNP bipolar transistor T.sub.12 and the zener diode Z.sub.2 through common discharge line 330 to the first resistor R.sub.a1 and the zener diode Z.sub.1. Therefore, the diode is not necessary in the present invention.

FIG. 4 shows another embodiment of the present invention, which is very similar to the previous embodiment but with different placement of the zener diodes also for the purpose of reducing the triggering voltage of SCR devices for CDL ESD protection circuitry. The zener diodes Z.sub.1, Z.sub.2 and Z.sub.n of the present embodiment are placed across the collectors and the emitters of the NPN bipolar transistors T.sub.21, T.sub.22 and T.sub.2n. That is, anodes of the zener diodes are connected to the second ends 306, 316 and 326 of the second resistors R.sub.b1, R.sub.b2 and R.sub.bn, and cathodes of the zener diodes are connected to the common discharge line 330.

In conclusion, a semiconductor device having the electrostatic discharge protective circuitry adapted to a common discharge line (CDL) is disclosed by the present invention with two embodiments. Wherein, the intrinsic symmetrical characteristics of discharge path in accompanies with the simplification in ESD protection design of using CDL structure have been brought into practice fully in ESD protection design by the present invention.

Of course, it is possible to apply the present invention to the ESD protection network with a SCR, and also it is possible for the present invention to protect any one ESD circuit and effectively making submicron IC devices immune to ESD damage. Also, this invention can be applied to provide the SCR with the zener diodes concerning ESD protection circuit used for protecting the devices has not been developed at present. The ESD structure of the present invention is the best integrated circuit structure.

Obviously, many modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the present invention may be practiced other than as specifically described herein.

Although specific embodiments have been illustrated and described, it will be obvious to those skilled in the art that various modifications may be made without departing from what is intended to be limited solely by the appended claims.